IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: William R. Wheeler et al.	Art Unit: 2812
Serial No.	: 09/941,158	Examiner:
Filed	: August 28, 2001	Stacy Whitmore
Assignee	: Intel Corporation	
Title	: MODEL-BASED LOGIC DESIGN	

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P.O. Box 1450
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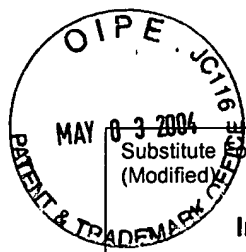Account No. 06-1050.

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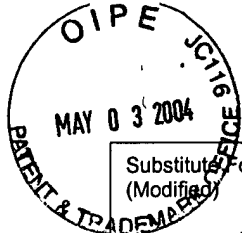Attorney for Intel Corporation

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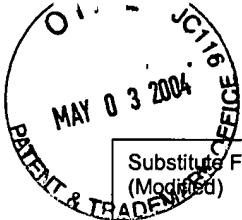| Substitute Form PTO-1449 (Modified) (37 CFR §1.98(b))	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-596001	Application No. 09/941,158
Information Disclosure Statement by Applicant (Use several sheets if necessary)		Applicant William R. Wheeler et al.	
		Filing Date August 28, 2001	Group Art Unit 2812

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	RE 38,059	04/2003	Yano, et al.			
	AB	4,703,435	10/1987	Darringer, et al.			
	AC	4,970,664	11/1990	Kaiser, et al.			
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	AAA	5,831,869	11/1998	Ellis, et al.			

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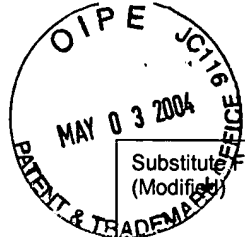
Substitute Disclosure Form (PTO-1449)

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	AOOO	2003/0177455	09/2003	Kaufman, et al.			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	No
	APPP	0 404 482	12/1990	EPO				
	AQQQ	0 720 233	07/1996	EPO				
	ARRR	0 901 088	03/1999	EPO				
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	AVVV	08-314892	11/1996	Japan				
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	AYYY	WO 98/55879	12/1998	WIPO				
	AZZZ	WO 99/39268	08/1999	WIPO				

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Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AAAAA	Gassenfeit, E. H., "Control System Design Realization via VHDL-A: Requirements", Proceedings of the 1996 IEEE International Symposium on Computer-Aided Control System Design, September 15, 1996, pp. 282-285.
	ABBBB	Kutzschebauch, "Efficient logic optimization using regularity extraction", Proceedings of 2000 International Conference on Computer Design, September 17, 2000, pp. 487-493.
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	ADDDD	Lin, et al., "A Goal Tree Based High-Level Test Planning System for DSP Real Number Models", 1998 Proceedings of International Test Conference, October 18, 1998, pp. 1000-1009.
	AEEEE	Maxfield, C., "Digital Logic Simulation: Event-Driven, Cycle-Based, and Home-Brewed", *Electrical Design News*, 41(14):129-136 (1996).
	AFFFF	NB84035598, "Binary Relational Schema to Model Structured LSI Design", IBM Technical Disclosure Bulletin, Vol. 26, No. 10B, March 1984, pp. 5598-5601.
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	AHHHH	NN8006341, "Macro Physical-To-Logical Checking LSI Chip Design", IBM Technical Disclosure Bulletin, Vol. 23, No. 1, June 1980, pp. 341-345.
	AIIII	NN9407481, "Functional Modeling using object Collaboration Diagram", IBM Technical Disclosure Bulletin, Vol. 37, No. 7, July 1994, pp. 481-486.
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	AKKKK	Su, Stephen, "An Interactive Design Automation System", *Proceedings of the 10th Design Automation Workshop on Design Automation*, pp. 253-261, June 1973
	ALLLL	Yli-Pietila, et al., "The Design and Simulation of Complex Multitechnology Systems", IEEE International Conference on Systems Engineering, August 9, 1990, pp. 474-477.

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